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EXAMINER	
ETTEHADIEH, ASLAN	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/681,951	**Applicant(s)** KIM ET AL.	
	Examiner Aslan Ettehadieh	**Art Unit** 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's cancellation of claim 10 in the reply filed on 06/07/2007 is acknowledged. Claim 10 is now cancelled. Office action address claims 1 – 9 and 11 – 12.

Response to Arguments

2. Applicant's arguments filed 06/07/2007 have been fully considered but they are not persuasive.

3. Applicant's arguments regarding claim 1, *Molloy does not disclose a controller including a PLL or DLL for de-multiplying the clocks signals of the oscillator.* Contrary to applicant's assertion, Molloy discloses a controller including a PLL or DLL for de-multiplying the clocks signals of the oscillator (figure 1 elements 106 – 112 comprise a PLL, further element 106 perform the function of de-multiplying (dividing) the clocks signals of the oscillator).

4. Applicant's arguments regarding claim 9, *Molloy does not disclose de-multiplying the clock signals of the oscillator by a predetermined number of times, and reading the MPEG data from the FIFO section in synchronization with the de-multiplied clock signals.* Contrary to applicant's assertion, Molloy discloses de-multiplying the clock signals of the oscillator by a predetermined number of times, and reading the MPEG data from the FIFO section in synchronization with the de-multiplied clock signals (figure 1 elements 106 – 112 comprise a PLL, further element 106 perform the function of de-multiplying (dividing) the clocks signals of the oscillator, the predetermined number of

times is interpreted broadly, where predetermined number of times can be interpreted as a value of "0", which means this limitation does not occur, the predetermined number of times could also be a value of "1" which is also taught by Molloy because the demultiplying is occurring, the predetermined number of times could also be a value of "2" which is also taught by Molloy because the system is continuous).

Claim Objections

5. Claims 11 – 12 are objected to because of the following informalities: Examiner believes that claim 11 was meant to be amended to be dependant to claim 9, not claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molloy (US 5337334) in view of Wei (US 2002/0154640).

2. Regarding claim 1, Molloy discloses an asynchronous transport stream receiver of a digital broadcasting receiving system comprising: a FIFO section for storing data; an oscillator for generating clock signals; a controller for reading and outputting the data stored in the FIFO section in synchronization with the clock signals of the oscillator, the controller including a PLL (Phase Locked Loop) or DLL (Dynamic Linking Library) for demultiplying the clock signals of the oscillator (col. 3 line 24 – col. 5 line 26; figure 1;

wherein elements 106 – 112 comprise a PLL, further element 106 perform the function of de-multiplying (dividing) the clocks signals of the oscillator; where an elastic store is being interpreted as a FIFO). Molloy is not explicit about MPEG data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode.

In the same field of endeavor, however, Wei discloses a FIFO section for storing MPEG data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode (abstract, paragraphs 1 – 3, 12, 22, 27, 28).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a FIFO section for storing MPEG data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode as taught by Wei in the system of Molloy to provide synchronization more easily (paragraph 2).

3. Regarding claim 2, Molloy further discloses wherein the controller is operative to demultiply the clock signals of the oscillator by a predetermined times and is synchronized with the demultiplied clock signals (figure 1 elements 107, 108, col. 4 lines 28 – 67; where a divider is being interpreted as a demultplying function).

4. Regarding claim 7, Molloy does not explicitly disclose the controller is an FPGA (Field Programmable Gate Array), however, it would have been obvious to one skilled in the art at the time of invention was made to use a controller designed in a FPGA in the system of Molloy to allow the controller to be reprogrammed or replaced without having to reprogram or replace the entire system, and also this applies to upgrading the actual FPGA to have a FPGA with a larger cell count allowing the controller to later be programmed to handle more system functionality.

5. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molloy (US 5337334) in view of Wei (US 2002/0154640) in view of Venkata et al. (US 2003/0052709) in further view of Prasad et al. (US 6298387).

6. Regarding claim 3, Molloy does not disclose a comparator for detecting sync byte; a counter for counting the MPEG data in terms of a packet unit of 188 bytes; and an MPEG data state decider for deciding a state of the MPEG data outputted from the FIFO section.

In the same field of endeavor, however, Venkata discloses a comparator for detecting sync byte and an video (paragraph 67) data state decider for deciding a state of the video data outputted from the FIFO section (figure 4, paragraphs 40 – 43, 45).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a comparator for detecting sync byte and an video data state decider for deciding a state of the video data outputted from the FIFO section as taught by Venkata in the system of Molloy to provide proper synchronization.

In the same field of endeavor, however, Prasad discloses a counter for counting the MPEG data in terms of a packet unit of 188 bytes (col. 1 lines 38 – 57). Prasad also discloses a comparator for detecting sync byte (col. 3 lines 1 – 11).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use a counter for counting the MPEG data in terms of a packet unit of 188 bytes as taught by Prasad in the system of Molloy to help locate the sync byte and thus to have provide synchronization.

7. Regarding claim 4, Venkata further discloses wherein the MPEG data state decider outputs valid signals of the MPEG data if byte detected by the comparator is the sync byte (figure 3 elements 280, 480, paragraph 43; where the outputs of elements 280, 480 are signals generated that are de-skewed (reduced jitter) which is being interpreted as valid) and Prasad further discloses the sync byte is Ox47 byte (col. 1 line 34).

8. Regarding claim 5, Prasad further discloses wherein the counter is operative to check the MPEG data at least twice in terms of a packet unit of 188 bytes to ensure that the detected Ox47 byte is the sync byte (col. 1 lines 38 – 57).

9. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molloy (US 5337334) in view of Wei (US 2002/0154640) in view of Venkata et al. (US 2003/0052709) in view of Prasad et al. (US 6298387) in further view of Tang et al. (US 2002/0075980).

10. Regarding claim 6, Molloy does not disclose wherein the FIFO section generates a flag signal if the data stored therein is greater than a predetermined size.

In the same field of endeavor, however, Tang discloses the FIFO section generates a flag signal if the data stored therein is greater than a predetermined size (abstract, paragraphs 37, 50, 56).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use the FIFO section generates a flag signal if the data stored therein is greater than a predetermined size as taught by Tang in the system of Molloy to make sure under/over flow does not occur.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molloy (US 5337334) in view of Wei (US 2002/0154640) in further view of Ngai (US 20010021227).

12. Regarding claim 8, Molloy does not disclose the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator is forwarded to an SD or HD leveled MPEG decoder for a subsequent processing.

In the same field of endeavor, however, Ngai discloses the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator is forwarded to an SD or HD leveled MPEG decoder for a subsequent processing (paragraphs 1, 25).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use the MPEG data stored in the FIFO section in synchronization with the clock signals of the oscillator is forwarded to an SD or HD leveled MPEG decoder for a subsequent processing as taught by Ngai in the system of Molloy to make sure the decoder is not overflowed (paragraph 25).

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkata et al. (US 2003/0052709) in view of Hui et al. (US 6868091).

14. Regarding claim 9, Venkata discloses a method for transmitting an asynchronous transport stream of a digital broadcasting receiving system having an FIFO section for storing video data generated based on a DVB-ASI (Digital Video Broadcasting Asynchronous Serial Interface) mode and an oscillator for generating clock signals, the method comprising the steps of: detecting (paragraph 40 – 43; where reading is being interpreted as detecting) whether the video data (paragraph 67) is stored in the FIFO

section (paragrapghs 34, 40 – 43, 102, 104, figure 4 elements 220, 420; where it is well known to one skilled in the art at the time of invention was made that a FIFO being controlled with a synchronization device (in this case a PLL, but also can be a DLL) with read/write control with use of flag signals for example (paragraph 34), i.e. half full flag, half empty flag; to indicate a FIFO fill level to be use filling/writing the FIFO and emptying/reading from the FIFO to provide the system no to over or under flow. Evidence cited by references below in *Other prior art cited* section); if detected, retrieving the video data from the FIFO section in synchronization with the clock signals of the oscillator (paragraphs 40 – 43, figure 4 elements 102, 104; where the PLL is well known to one skilled in the art at the time of invention was made to have an oscillator, i.e. a VCO or NCO), de-multiplying the clock signals of the oscillator by a predetermined number of times, and reading the MPEG data from the FIFO section in synchronization with the de-multiplied clock signals (figure 1 elements 106 – 112 comprise a PLL, further element 106 perform the function of de-multiplying (dividing) the clocks signals of the oscillator, the predetermined number of times is interpreted broadly, where predetermined number of times can be interpreted as a value of "0", which means this limitation does not occur, the predetermined number of times could also be a value of "1" which is also taught by Molloy because the de-multiplying is occurring, the predetermined number of times could also be a value of "2" which is also taught by Molloy because the system is continuous); detecting sync byte from the retrieved video data (figure 4 elements 250, 450, paragraphs 42 – 43); and generating valid signals indicative of the video data when the sync byte is detected (figure 3 elements 280, 480, paragraph 43; where the outputs of elements 280, 480 are signals generated that are de-skewed (reduced jitter) which is being interpreted as valid). Venkata does not explicitly disclose MPEG.

In the same field of endeavor, however, Hui discloses MPEG (col. 1 lines 13 – 67, col. 2 lines 46 – 55). Hui also discloses detecting a sync word from the retrieved MPEG data of the FIFO (figure 1, col. 1 lines 13 – 67, col. 2 lines 46 – 55).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use MPEG as taught by Hui in the system of Venkata because of MPEG compression capabilities.

15. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkata et al. (US 2003/0052709) in view of Hui et al. (US 6868091) in further view of Roy et al. (US 2001/0016023).

16. Regarding claim 10, Venkata discloses a PLL (figure 4 elements 104, 102; where PLL are well known to one skilled in the art at the time of invention was made to include a phase detector/comparator, a loop filter, oscillator, and a divider). Venkata does disclose reading the Video data from the FIFO section in synchronization with the PLL (paragraphs 38, 40 – 43). Venkata is not explicit about the inter-working of the PLL.

In the same field of endeavor, however, Roy discloses demultplying the clock signals of the oscillator by a predetermined times and reading data from the FIFO section in synchronization with the demultiplied clock signals (figure 15, paragraph 111; where the receive elastic store is being interpreted as a FIFO and element 1560, a divider, is being interpreted as a demultplying function).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use demultplying the clock signals of the oscillator by a predetermined times and reading data from the FIFO section in synchronization with the demultiplied clock signals as taught by Roy in the system of Venkata to reduce jitter (paragraph 106).

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkata et al. (US 2003/0052709) in view of Hui et al. (US 6868091) in view of Roy et al. (US 2001/0016023) in further view of Takashi et al. (US 2003/0028820).

18. Regarding claim 11, Venkata is not explicit about wherein the detecting step of sync byte sets the FIFO section into a read state.

In the same field of endeavor, however, Takashi discloses wherein the detecting step of sync byte sets the FIFO section into a read state (paragraph 113).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use wherein the detecting step of sync byte sets the FIFO section into a read state as taught by Takashi in the system of Venkata to provide synchronization (paragraph 113)..

19. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkata et al. (US 2003/0052709) in view of Hui et al. (US 6868091) in further view of Roy et al. (US 2001/0016023) in further view of Matsumura et al. (US 2001/0004366).

20. Regarding claim 12, the above rejection disclosed detecting the sync byte from the MPEG data, however, Venkata in view of Hui in further view of Roy does not

disclose the sync byte being 0x47, and checking whether the Ox47 byte is sync byte using a counter.

In the same field of endeavor, however, Matsumura discloses the sync byte being 0x47, and checking whether the Ox47 byte is sync byte using a counter (paragraphs 90, 92, 98 – 101, 139).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use the sync byte being 0x47, and checking whether the Ox47 byte is sync byte using a counter as taught by Matsumura in the system of Venkata to provide synchronization (paragraph 139).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aslan Ettehadieh
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